Enrollment No: _____ Exam Seat No:_____

C. U. SHAH UNIVERSITY

Winter Examination-2019

Subject Name: VLSI Technology

Subject Code: 4TE07VLT1 **Branch: B.Tech (EC)**

Semester: 7 **Date : 15/11/2019** **Time : 10:30 To 01:30** **Marks : 70**

Instructions:

(1) Use of Programmable calculator & any other electronic instrument is prohibited.
(2) Instructions written on main answer book are strictly to be obeyed.
(3) Draw neat diagrams and figures (if necessary) at right places.
(4) Assume suitable data if needed.

Q-1 **Attempt the following questions** **(14)**

a) Draw the Y-chart for VLSI design flow in three domains.
b) Define the term semi custom design style.
c) Define the term full custom design style.
d) State the different criteria used for measure the design quality for chip design.
e) Define the term photo lithography.
f) Define the terms positive photo-resist
g) Define the terms negative photo-resist.
h) Define the terms Enhancement and Depletion mode MOSFET.
i) State the type of Fermi level potential for n-type and p-type silicon substrate.
j) Define the term work function.
k) Define the term threshold voltage $V_{TO.}$
l) Define the term controllability.
m) Define the term obsrevability.
n) Define the term testability.

Attempt any four questions from Q-2 to Q-8

Q-2 **Attempt all questions** **(14)**

a) Discuss following approaches (with examples) used to reduce complexity of IC design: 1. Hierarchy, 2. Regularity, 3. Modularity, and 4. Locality. **07**

b) Why do we need isolation between MOS transistors fabricated on a single chip? Explain etched field-oxide isolation and LOCOS isolation techniques with diagrams. **07**

Q-3 **Attempt all questions** **(14)**

a) Explain the band diagram of MOS Structure at surface inversion and derive the expression for threshold voltage. **07**

b) What is the need of scaling? Discuss constant voltage scaling in detail with its merits and demerits. **07**

Q-4 **Attempt all questions** **(14)**

a) Draw and explain the CMOS inverter. Find the V_{IL}, V_{IH} and V_{th} equation for **07**

CMOS inverter.

	b)	Draw the combinational logic circuit using NMOS for the following Boolean expression: (i)Y1 = (AB + CD + E)’ (ii) Y2= (A(D + E) + BC)’	**07**
Q-5		**Attempt all questions**	**(14)**
	a)	Explain the estimation of interconnect parasitic.	**07**
	b)	Discuss the effect of charge storage and charge leakage in pass transistor circuits.	**07**
Q-6		**Attempt all questions**	**(14)**
	a)	Explain in detail SR latch circuit.	**07**
	b)	Explain in detail CMOS D-latch and edged triggered flip flop.	**07**
Q-7		**Attempt all questions**	**(14)**
	a)	Explain CMOS transmission gate logic.	**07**
	b)	Explain Latch up problem in CMOS inverter. Mention causes and remedy for avoiding latch up.	**07**
Q-8		**Attempt all questions**	**(14)**
	a)	Write short note on Fault types and models.	**07**
	b)	Discuss various packaging technology used for VLSI chips.	**07**